APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,787	12/02/2003	Michael J. Koster	SUN-P8985-SPL	6112

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EXAMINER
THOMAS, SHANE M

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/726,787	KOSTER ET AL.
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-10,12 and 14-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-10,12 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003 and 17 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 7/17/2006. Claims 1,3,5-1,12,

and 14-20 remain pending; claims 2,4,11 and 13 have been canceled. Applicants' amendment

and accompanying arguments have been carefully considered, but they are not persuasive and do

not place the claims in condition for allowance. Accordingly, this action has been made FINAL.

All previously outstanding objections and rejections to the Applicant's disclosure and

claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Response to Amendment/Arguments

Applicant has amended independent claims 1,10,19, and 20, to state that the initializing,

monitoring, and the switching, is performed within the cache controller in the processor. While

the embodiment associated with figure 1 of Ang is discussed in detail throughout the reference,

Ang states in ¶61-63 that in another embodiment of the invention, instead of taking place

between the L2 cache and the L3 cache of figure 1, the teachings of the invention may be

practiced between the L1 cache and the L2 cache - both shown as being contained within the

processor 102 (figure 1). As the invention may be practiced between the L1 and L2 caches (or

any hierarchical cache system as taught in ¶63) instead of the L2 and L3 caches of Ang, it can be

seen that Ang teaches the amended limitations. Because Ang teaches that the L1 and L2 caches

are contained within processor 102, it follows that the L2 cache controller would thereby

incorporate the functionality of the memory controller 106; therefore the steps of initializing,

monitoring, and switching may be performed by the (L2) cache controller in the processor 102.

It follows that the processor 102 therefore may be equipped with an initialization mechanism, a

monitoring mechanism, and a protocol switching mechanism, which may all be contained in the

L2 cache controller (¶62).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3,5,6,8-12,14,15, and 17-20 are rejected under 35 U.S.C. 102(e) as being

anticipated by Ang (U.S. Patent Application Publication No. 2003/0079085).

As per claims 1,10, and 20, Ang teaches **initializing a cache to operate using a write-**

invalidate protocol (¶20), monitoring a dynamic behavior of the cache during program

execution (¶65), wherein monitoring the dynamic behavior of the cache involves

maintaining a count for each cache line of the number of cache line invalidations the cache

line has been subject to during program execution and if the dynamic behavior indicated

that better performance can be achieved using a wrote-broadcast protocol, switching the

cache to operate using the write-broadcast protocol (¶48). In ¶48, Ang teaches when deciding

to transition from the invalidation to the update protocol, which is known in the art to be

synonymous with the write-broadcast protocol (¶3), the memory-side coherence engine tracks

the frequency (i.e. the number of occurrences, thereby which a counter is inherent) of cache-line

invalidations. When the frequency of the invalidations reaches a threshold, the cache coherence

protocol is dynamically switched from a write-invalidation scheme to a write-update (or write-broadcast) scheme.

As discussed above in the Response to Amendments section, the steps of **initializing, monitoring and switching** may be **performed by the cache controller** <u>in the processor</u> 102 (¶¶61-63 of Ang).

As per claims 3 and 12, Ang teaches **switching to the write-broadcast** (i.e. the write-update) **protocol on a cache-line by cache-line basis** (¶48).

As per claims 5 and 14, Ang teaches **if the number of cache line invalidations indicates that a given cache line is updated frequently, switching the cache line to operate under the write-broadcast protocol** (write-update) in ¶48. Specifically, Ang teaches if the frequency of invalidations for a particular cache-line is frequent (i.e. above an inherent threshold), then the coherency policy for that particular cache line is changed to a write-update policy.

As per claims 6 and 15, Ang teaches **wherein if a given cache line is using the write-broadcast protocol and the number of cache line updates indicates that the given cache line is not being contended for by multiple processors** (i.e. only one processor is updating the cache line, as specifically claimed in claim 15), **switching the given cache line back the write-invalidation protocol** (¶48).

As per claims 8 and 17, Ang teaches **the** [processor implementing a] **write-invalidate protocol sends an invalidation message to other caches in a shared memory multiprocessor when a given cache line is updated in a local cache** (¶20). Further the Applicant's Admitted Prior Art (herein "APA") teaches that such a limitation is inherent in write-invalidation protocols (¶6 of Applicant's specification).

As per claims 9 and 18, Ang teaches **the** [processor implementing a] **write-broadcast**

protocol broadcasts an update to other caches in a shared memory multiprocessor when

the given cache line is updated in a local cache (¶3). Further, the APA teaches that such a

limitation is inherent in write-broadcast (i.e. write-updating) protocols (¶9).

As per claim 19, the rejection follows the rejection for claims 1, 10, and 20 set forth

above. Further, Ang teaches **a plurality of processors** (abstract, and labeled 102 in figure 1),

wherein a processor within the plurality of processors includes a cache 122, a shared

memory 108, and a bus (connection shown in figure 1 between the network and between

controller 106 of the node to the shared memory 108) **coupled between the plurality of**

processors and the shared memory, wherein the bus transports addresses and data between

the shared memory and the plurality of processor (necessarily inherent in the system of Ang

as it is well known in the art that in order to access a location in a memory, an address is required

and in order to receive requested data, the data must be retrieved from the memory and sent back

to the requesting processor/hardware unit).

As discussed above in the Response to Amendments section, the steps of **initializing,**

monitoring and switching may be **performed by the cache controller in the processor** 102

(¶¶61-63 of Ang).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ang (U.S.

Patent Application Publication No. 2003/0079085), as applied to claims 1-3,5,6,8-12,14,15, and

17-20, above.

As per claims 7 and 16, Ang does not specifically teach **wherein if a shared memory**

multiprocessor includes modules that are not able to switch to the write-broadcast

protocol, locking the cache into the write-invalidate protocol; however, such a limitation

would have been obvious to one having ordinary skill in the art at the time the invention was

made, as a given processor operating in the write-invalidate mode amongst other processors of a

shared memory multiprocessor system operating in a write-update mode would pose a data

integrity issue. Such obviousness is best set forth via an example. If cache line address A is

currently shared among a first processor operating in a write-broadcast mode a second processor

in a write-invalidate mode and the first processor modified address A, the first processor would

also send out the updated data associated with address A (as discussed in the write-update

protocol definition in Ang ¶3 and Applicant's ¶9). The second processor, not operating in the

write-update mode would never receive the updated data (as it only awaits for invalidation

messages to notify of shared cache line modifications) and instead assumes the data associated

with address A contained within its local cache is still valid. Therefore, when the second

processor attempts to read from its local cache line address A, the data, as appears to the shared

memory, is invalid as the first processor had already updated this data. Thus the data read by

processor from its local cache would have been invalid.

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to have combined the cache coherency protocol of Ang by locking the

multiprocessor caches into a write-invalidate mode, if the cache (or portion thereof) of a

particular processor of the multiprocessor shared memory system was not capable of switching

to a write-broadcast protocol, thereby maintaining data integrity by way of keeping the caching

policies among the plurality of processors in the multiprocessor shared memory system coherent

with each other.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188.

The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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